1.25Gbps CWDM SFP, DDMI, LC

Features

- Operating data rate up to 1.25Gbps
- 16-Wavelength CWDM DFB LD Transmitter from 1310 nm to 1610 nm, with step 20 nm
- APD High Sensitivity Receiver
- 41 dB Power Budget
- Duplex LC Connector Interface
- Hot Pluggable
- Compliant with MSA SFP Specification
- Digital diagnostic monitor interface
- Compatible with SFF-8472

Applications

- Gigabit Ethernet Switches and Routers
- Other Optical Link

CWDM* Wavelength (0 to 70°C)

band	Nomenclature	Wavelength(nm)		
		Min.	Typ.	Max.
O-band Original	C	1304	1310	1317.5
	D	1324	1330	1337.5
	E	1344	1350	1357.5
E-band Extended	F	1364	1370	1377.5
	G	1384	1390	1397.5
	H	1404	1410	1417.5
	I	1424	1430	1437.5
	J	1444	1450	1457.5
S-band Short Wavelength	K	1464	1470	1477.5
	L	1484	1490	1497.5
	M	1504	1510	1517.5
	N	1524	1530	1537.5
C-band Conventional	O	1544	1550	1557.5
L-band Long Wavelength	P	1564	1570	1577.5
	Q	1584	1590	1597.5

	R	1604	1610	1617.5

CWDM*: 16 Wavelengths from 1310 nm to 1610 nm, each step 20 nm.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	+85	°C
Supply Voltage	V_{CC}	-0.5	3.6	V

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T_A	0		+70	°C
		-40		+85	
Power Supply Voltage	V_{CC}	3.15	3.3	3.45	V
Power Supply Current	I_{CC}			300	mA
Data Rate			1.25		Gbps

PERFORMANCE SPECIFICATIONS - ELECTRICAL

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
TRANSMITTER						
LVPECL Inputs(Differential)	Vin	400		2000	mVp	AC coupled inputs*(note1)
Input Impedance (Differential)	Zin	85	100	115	ohms	Rin > 100 kohms @ DC
Tx_DISABLE Input Voltage - High		2		Vcc	V	
Tx_DISABLE Input Voltage - Low		0		0.8	V	
Tx_FAULT Output Voltage -- High		2		Vcc+0.3	V	
Tx_FAULT Output Voltage -- Low		0		0.5	V	
RECEIVER						
LVPECL Outputs (Differential)	Vout	370		2000	mVpp	AC coupled outputs*(note1)
Output Impedance (Differential)	Zout	85	100	115	ohms	
Rx_LOS Output Voltage - High		2		Vcc+0.3	V	
Rx_LOS Output Voltage - Low		0		0.8	V	
MOD_DEF (0:2)	VoH	2.5			V	With Serial ID
	VoL	0		0.5	V	

Optical and Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit
Data Rate			1.25		Gbps
Transmitter					
Centre Wavelength	λ_C	λc–5.5	λc	λc+7.5	nm
Spectral Width (-20dB)	σ			1	nm
Average Output Power*(note2)	P_{0ut}	+5		+8	dBm
Extinction Ratio*(note3)	EX	8.2			dB
Side Mode Suppression Ratio	SMSR	30			dB
Rise/Fall Time(20% ~ 80%)	tr/tf			0.26	ns
Total Jitter	TJ			56.5	ps
Pout@TX Disable Asserted	Pout			-45	dBm
TX_Disable Assert Time	t_off			10	us
Output Optical Eye*(note3)	IEEE802.3ah Compliant*(note6)				
Receiver					
Centre Wavelength	λ_C	1260		1600	nm
Receiver Sensitivity*(note4)	Pmin			-36	dBm
Receiver Overload	Pmax	-9			dBm
Return Loss		12			dB
Optical Path Penalty*(note5)				1	dB
LOS De-Assert	LOSD			-37	dBm
LOS Assert	LOSA	-45			dBm
LOS Hysteresis*(note7)		1			dB

Note 1: LVPECL logic, internally AC coupled.

Note 2: Output is coupled into a 9/125μm single-mode fiber.

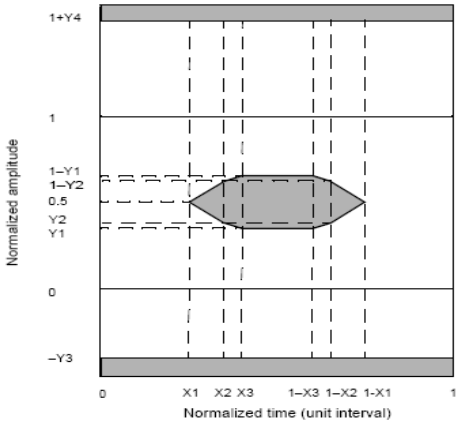
Note 3: Filtered, measured with a PRBS 2^7-1 test pattern @1.25Gbps

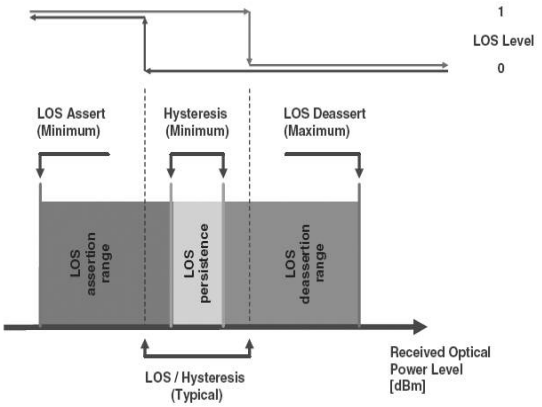
Note 4: Minimum average optical power measured at BER less than 1E-12, with a 2^7-1 PRBS and ER=9dB.

Note 5: Measured with a PRBS 2^7-1 test pattern @1.25Gbps, BER ≤1×10^{-12}.

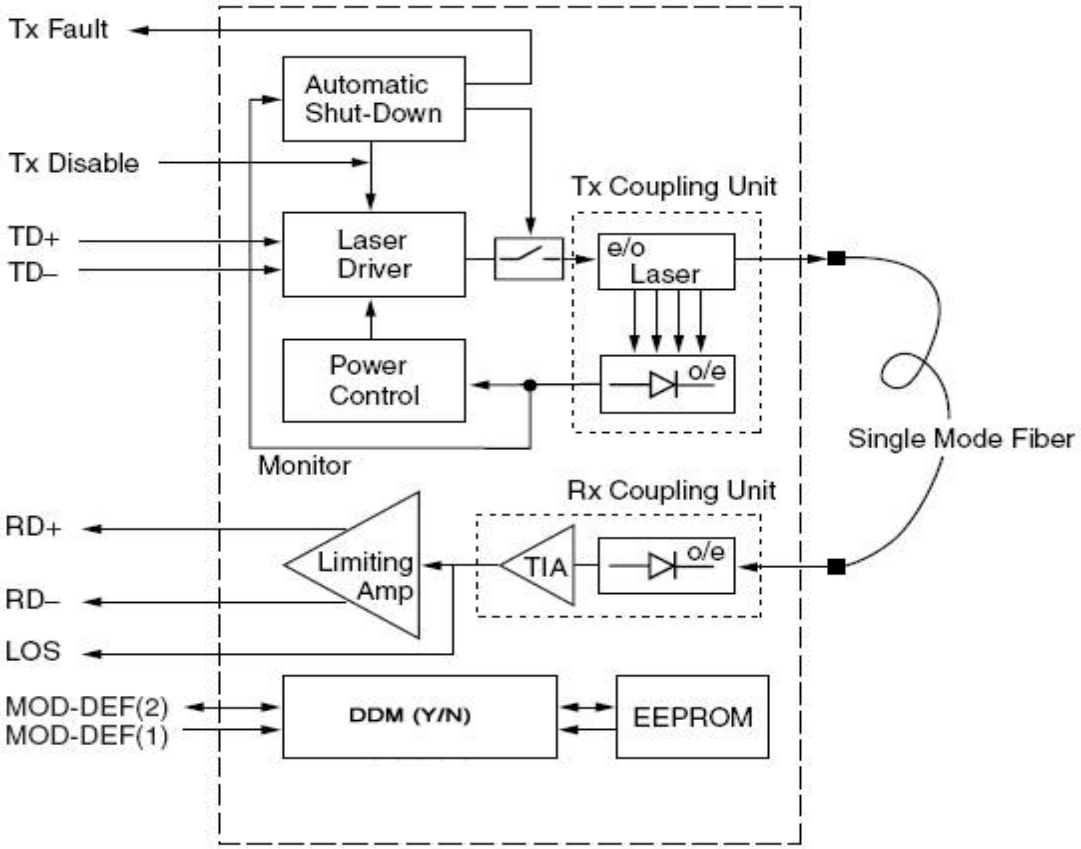
Note 6: Eye pattern mask

Note 7: LOS Hysteresis

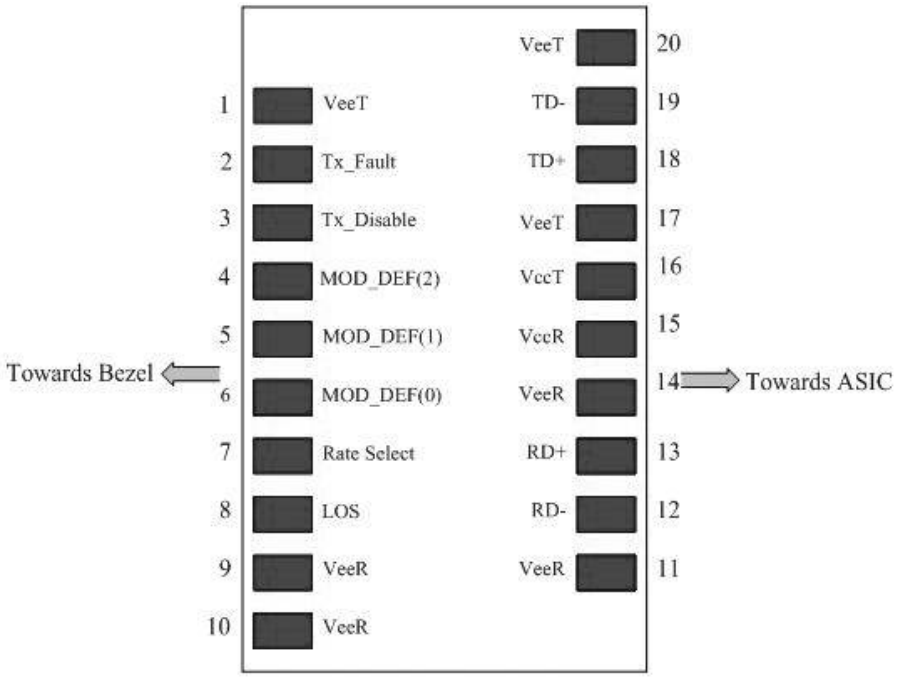


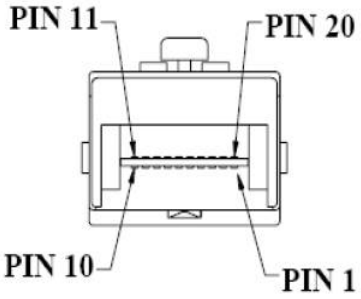


Functional Description of Transceiver



SFP Transceiver Electrical Pad Layout





Pin Function Definitions

Pin Num.	Name	FUNCTION	Plug Seq.	Notes
1	VeeT	Transmitter Ground	1	
2	TX Fault	Transmitter Fault Indication	3	Note 1
3	TX Disable	Transmitter Disable	3	Note 2, Module disables on high or open
4	MOD-DEF2	Module Definition 2	3	Note 3, Data line for Serial ID.

5	MOD-DEF1	Module Definition 1	3	Note 3, Clock line for Serial ID.
6	MOD-DEF0	Module Definition 0	3	Note 3, Grounded within the module.
7	Rate Select	Not Connect	3	Function not available
8	LOS	Loss of Signal	3	Note 4
9	VeeR	Receiver Ground	1	Note 5
10	VeeR	Receiver Ground	1	Note 5
11	VeeR	Receiver Ground	1	Note 5
12	RD-	Inv. Received Data Out	3	Note 6
13	RD+	Received Data Out	3	Note 7
14	VeeR	Receiver Ground	1	Note 5
15	VccR	Receiver Power	2	3.3 ± 5%, Note 7
16	VccT	Transmitter Power	2	3.3 ± 5%, Note 7
17	VeeT	Transmitter Ground	1	Note 5
18	TD+	Transmit Data In	3	Note 8
19	TD-	Inv. Transmit Data In	3	Note 8
20	VeeT	Transmitter Ground	1	Note 5

Notes:

1) TX Fault is an open collector/drain output, which should be pulled up with a 4.7K – 10KΩ resistor on the host board. Pull up voltage between 2.0V and VccT, R+0.3V. When high, output indicates a laser fault of some kind. Low indicates normal operation. In the low state, the output will be pulled to < 0.8V.

2) TX disable is an input that is used to shut down the transmitter optical output. It is pulled up within the module with a 4.7 – 10 K Ω resistor. Its states are:
Low (0 – 0.8V): Transmitter on
(>0.8, < 2.0V): Undefined
High (2.0 – 3.465V): Transmitter Disabled
Open: Transmitter Disabled

3) Mod-Def 0,1,2. These are the module definition pins. They should be pulled up with a 4.7K – 10KΩresistor on the host board. The pull-up voltage shall be VccT or VccR (see Section IV for further details). Mod-Def 0 is grounded by the module to indicate that the module is present Mod-Def 1 is the clock line of two wire serial interface for serial ID Mod-Def 2 is the data line of two wire serial interface for serial ID

4) LOS (Loss of Signal) is an open collector/drain output, which should be pulled up with a 4.7K – 10KΩ resistor. Pull up voltage between 2.0V and VccT, R+0.3V. When high, this output indicates the received optical power is below the worst-case receiver sensitivity (as defined by the standard in use). Low indicates normal operation. In the low state, the output will be pulled to < 0.8V.

5) VeeR and VeeT may be internally connected within the SFP module.

6) RD-/+: These are the differential receiver outputs. They are AC coupled 100Ω differential lines which should be terminated with 100Ω (differential) at the user SERDES. The AC coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines will be between 370 and 2000 mV differential (185 – 1000 mV single ended) when properly terminated.

7) VccR and VccT are the receiver and transmitter power supplies. They are defined as 3.3V ±5% at the SFP connector pin. Maximum supply current is 300mA. Recommended host board power supply filtering is shown below. Inductors with DC resistance of less than 1 ohm should be used in order to maintain the required voltage at the SFP input pin with 3.3V supply voltage. When the recommended supply-filtering network is used, hot plugging of the SFP transceiver module will result in an inrush current of no more than 30mA greater than the steady state value. VccR and VccT may be internally connected within the SFP transceiver module.

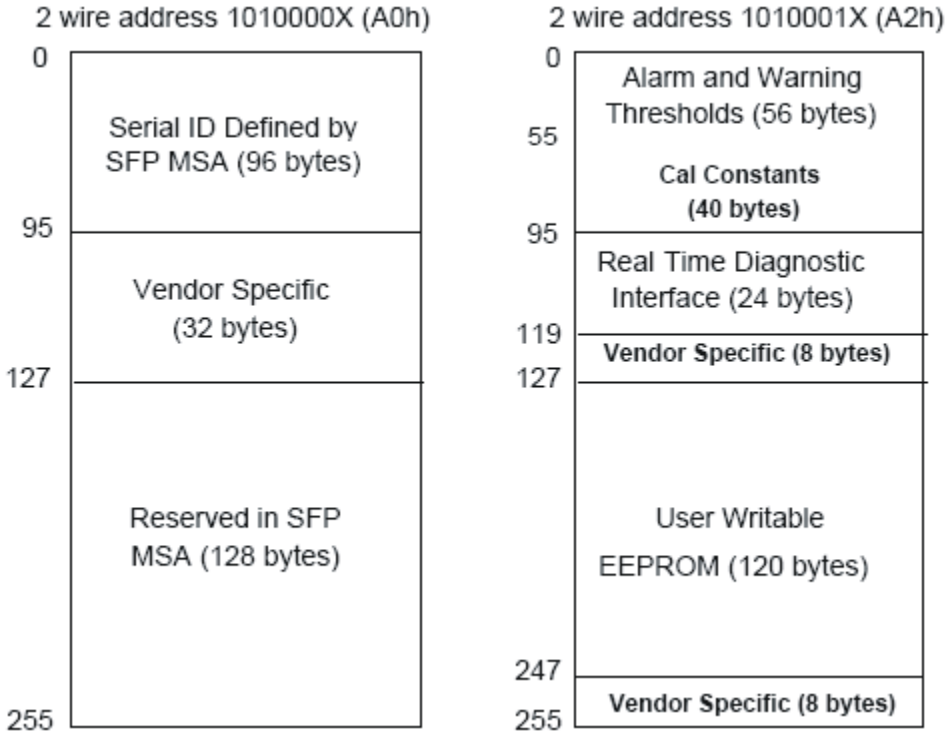
8) TD-/+: These are the differential transmitter inputs. They are AC-coupled, differential lines with 100Ω differential termination inside the module. The AC coupling is done inside the module and is thus not required on the host board. The inputs will accept differential swings of 500 – 2400 mV (250 – 1200mV single-ended), though it is recommended that values between 500 and 1200 mV differential (250 – 600mV single-ended) be used for best EMI performance.

EEPROM

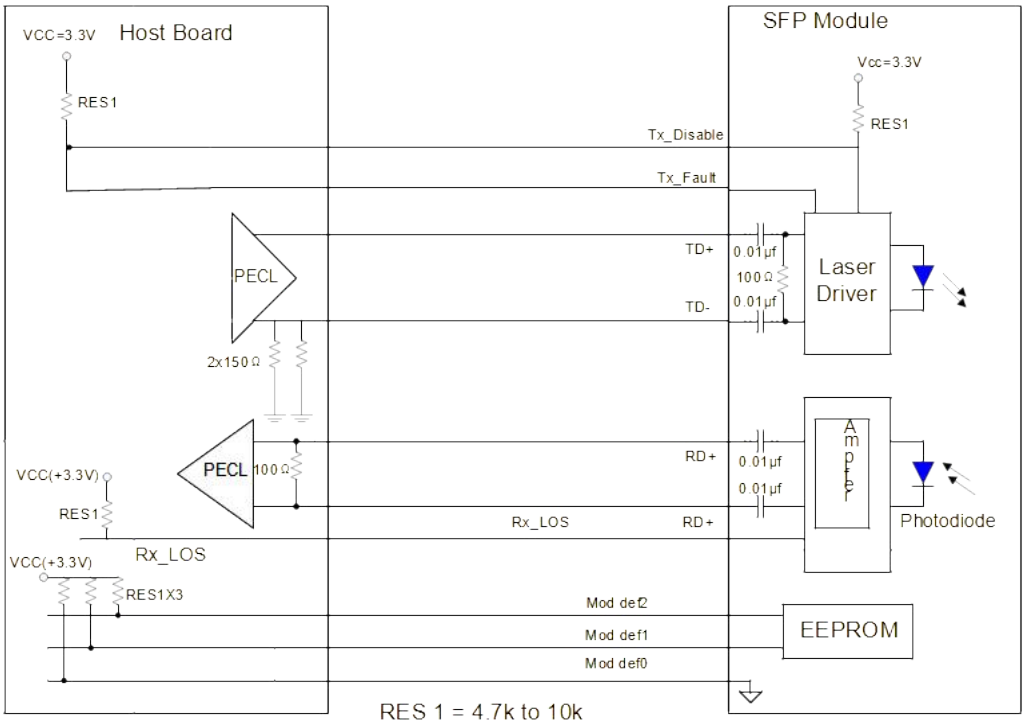
The serial interface uses the 2-wire serial CMOS EEPROM protocol defined for the ATMEL AT24C02/04 family of components. When the serial protocol is activated, the host generates the serial clock signal (SCL). The positive edge clocks data into those segments of the EEPROM that are not write protected within the SFP transceiver. The negative edge clocks data from the SFP transceiver. The serial data signal (SDA) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially.

The Module provides diagnostic information about the present operating conditions. The transceiver generates this diagnostic data by digitization of internal analog signals. Calibration and alarm/warning threshold data is written during device manufacture. Received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring all are implemented. The diagnostic data are raw A/D values and must be converted to real world units using calibration constants stored in EEPROM locations 56 – 95 at wire serial bus address A2h. The digital diagnostic

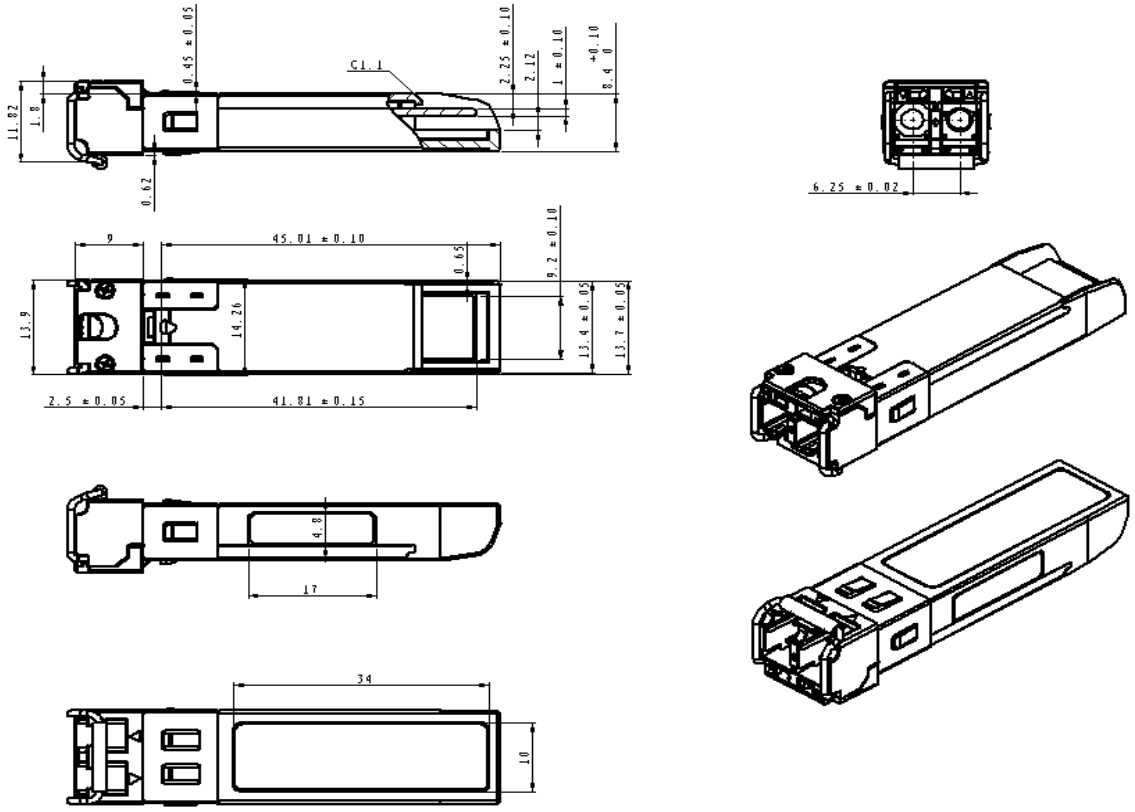
memory map specific data field define as following .For detail EEPROM information, please refer to the related document of SFF 8472 Rev 9.3



Recommend Circuit Schematic



Mechanical Specifications



Laser Emission