QSFP28, 100G, CWDM4, 2km, 2xLC

Особенности:
- Supports 103Gbps
- Single 3.3V Power Supply
- Power dissipation < 3.5W
- Up to 2km over SMF
- 4x25G electrical interface
- Duplex LC receptacles
- Commercial case temperature range of 0°C to 70°C
- 4*25Gbps DFB-based CWDM transmitter
- PIN and TIA array on the receiver side
- I2C interface with integrated Digital Diagnostic Monitoring

Области применения:
- 100G CLR4 applications with or without FEC

Part No.	Da-ta	Fiber	Distance *(note2)	Interface	Temp.	DDMI
QSFP28.100G.CWDM4-2 *(note1)	103Gbps	SMF	2km	LC	0℃~+70℃	Yes

Note1: also support 103Gbps Note2: Over SMF

*The product image only for reference purpose.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Operating Relative Humidity	RH	5	85	%
Receiver Damage Threshold, per Lane	Rxdmg	5.5		dBm

*Exceeding any one of these values may damage the device permanently.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	Tc	0	25	70	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Power Dissipation	P_D			3.5	W

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes

Transmitter						
Differential data input swing per lane				900	mv_{p-p}	
Input Impedance (Differential)	Zin			10	%	
Stressed input parameters						
Eye width		0.46			UI	
Applied pk-pk sinusoidal jitter		IEEE 802.3bm Table 88-13				
Eye height		95			mv	
DC common mode voltage		-350		2850	mv	
Receiver						
Differential output amplitude		200		900	mv_{p-p}	
Output Impedance (Differential)	Zout			10	%	
Output Rise/Fall Time	t_r/t_f	12			ps	20%~80%
Eye width		0.57			UI	
Eye height differential		228			mv	
Vertical eye closure				5.5	dB	

Optical Characteristics

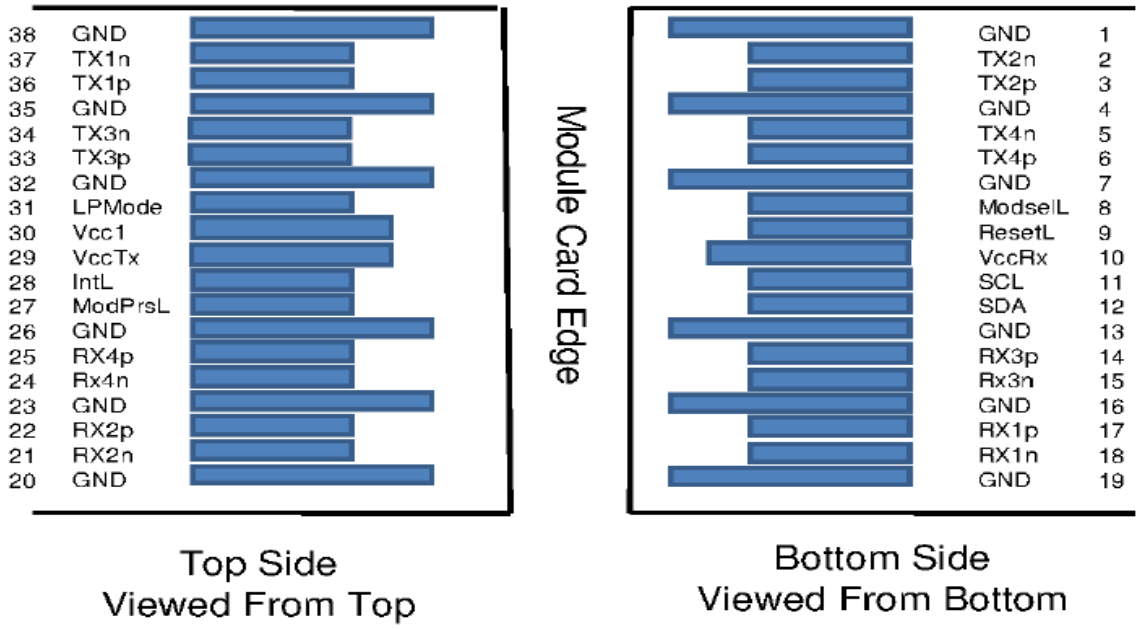
Parameter	Symbol	Min.	Typical	Max.	Unit
Transmitter					
Signaling Speed per Lane	BR_{AVE}		25.78		Gbps
Data Rate Variation		-100		+100	ppm
Lane_0 Center Wavelength	λ_{C0}	1264.5		1277.5	nm
Lane_1 Center Wavelength	λ_{C1}	1284.5		1297.5	nm
Lane_2 Center Wavelength	λ_{C2}	1304.5		1317.5	nm
Lane_3 Center Wavelength	λ_{C3}	1324.5		1337.5	nm
Total Average Output Power	Po			8.3	dBm
Average Launch Power each Lane*(Note3)	Peach	-6.5		2.3	dBm
Transmit OMA each Lane *(Note4)	TxOMA	-4.0		2.5	dBm
Launch power in OMA minus TDP, each lane	OMA-TDP	-5.0			dBm
Transmitter and Dispersion Penalty per Lane *(Note5)	TDP			3	dB
Average launch power of OFF transmitter, each lane	P_off			-30	dBm
Side Mode Suppression Ratio	SMSR	30			dB
Optical Return Loss Tolerance				20	dB
Transmitter Reflectance				-12	dB

*(Note6)					
Extinction Ratio	ER	3.5			dB
RIN OMA	RIN			-130	dB/Hz
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}*(Note7)		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			
Receiver					
Signaling Speed per Lane	BR_{AVE}		25.78		Gbps
Data Rate Variation		-100		+100	ppm
Damage threshold	Rxdmg	3.3			dBm
Lane_0 Center Wavelength	λ_{C0}	1264.5		1277.5	nm
Lane_1 Center Wavelength	λ_{C1}	1284.5		1297.5	nm
Lane_2 Center Wavelength	λ_{C2}	1304.5		1317.5	nm
Lane_3 Center Wavelength	λ_{C3}	1324.5		1337.5	nm
Average receive power *(Note8)	Rxpow	-10		2.3	dBm
Receive Power (OMA) per Lane	RxOMA			2.5	dBm
Unstressed Receiver Sensitivity (OMA) per Lane with FEC *(Note9)	Rxsens_FEC			-11	dBm
Unstressed Receiver Sensitivity (OMA) per Lane without FEC *(Note9)	Rxsens			-8.5	dBm
Stressed Receiver Sensitivity (OMA) per Lane with FEC *(Note10)	RXSRS_FEC			-8.5	dBm
Stressed Receiver Sensitivity (OMA) per Lane without FEC *(Note10)	RXSRS			-6	dBm
Optical Return Loss	ORL			-26	dB
Conditions of stressed receiver sensitivity test					
Vertical Eye Closure Penalty *(Note11)	VECP			2.5	dB
Stressed J2 Jitter with FEC *(Note11)	J2			TBD	UI
Stressed J4 Jitter with FEC *(Note11)	J4			TBD	UI
Stressed J2 Jitter without FEC *(Note12)	J2			0.3	UI
Stressed J9 Jitter without FEC *(Note12)	J9			0.47	UI
LOS Assert	LOSA	-25			dBm
LOS De-Assert	LOSD			-12	dBm
LOS Hysteresis		0.5			dB

Note3: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
Note4: Even if the TDP < 1.0dB, the OMA (min) must exceed this value.
Note5: TDP does not include a penalty for multi-path interference (MPI).
Note6: Transmitter reflectance is defined looking into the transmitter.
Note7: With FEC hit ratio of $5x10^{-5}$, Without FEC hit ratio of $1x10^{-12}$.
Note8: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
Note9: With FEC sensitivity is specified at $5x10^{-5}$ BER, Without FEC sensitivity is specified at $1x10^{-12}$ BER.

Note10: With FEC measured with conformance test signal at TP3 for BER = $5x10^{-5}$, Without FEC measured with conformance test signal at TP3 for BER = $1x10^{-12}$.
Note11: Vertical eye closure penalty, stressed eye J2 Jitter, stressed eye J4 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
Note12: Vertical eye closure penalty, stressed eye J2 Jitter, stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

QSFP28 Transceiver Electrical Pad Layout



Pin Function Definitions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	

16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

1: GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP28 Module in any combination. The connector pins are each rated for a maximum current of 500mA.

Mechanical Specifications