Соединитель, QSFP+ - 4 x SFP+, 30AWG, 1, 2, 3m

Особенности:

- Support 4 lanes of 10 Gb/s
- AC coupling of PECL signals
- 100 ohm differential impedance system
- Power Supply +3.3V
- Low Near-End Crosstalk
- Fully compatible with IEEE802.3ba
- Temperature Range -5 to 75°C
- All-metal housing for superior EMI performance
- Precision process control for minimization of pair-to-pair skew
- EEPROM for cable signature & system communications
- QSFP End Compliant SFF-8436
- SFP+ End Compliant SFF-8431, SFF-8432, SFF-8472
- RoHS6 compliant

Part No.	Description	Cable Length (m)	AWG
QSFP-SFP-DA-1m	QSFP+ - 4 x SFP+	1	30
QSFP-SFP-DA-2m	QSFP+ - 4 x SFP+	2	30
QSFP-SFP-DA-3m	QSFP+ - 4 x SFP+	3	30

Product Description

QSFP-SFP-DA-Xm series copper direct-attach cables are suitable for very short distances and offer a highly cost-effective way to establish a 40-Gigabit link between QSFP ports of 4 SFP+ switches within racks and across adjacent racks. These cables are used for 40GbE and Infniband standards, to maximize performance. This interconnect system is fully compliant with existing industry standard specifications such as the QSFP MSA and IBTA (InfiniBand Trade Association). The QSFP+ cables support the bandwidth transmission requirements as defined by IEEE 802.3ba (40 Gb/s) and Infiniband QDR (4x10 Gb/s per channel) specifications.

Absolute Maximum Ratings

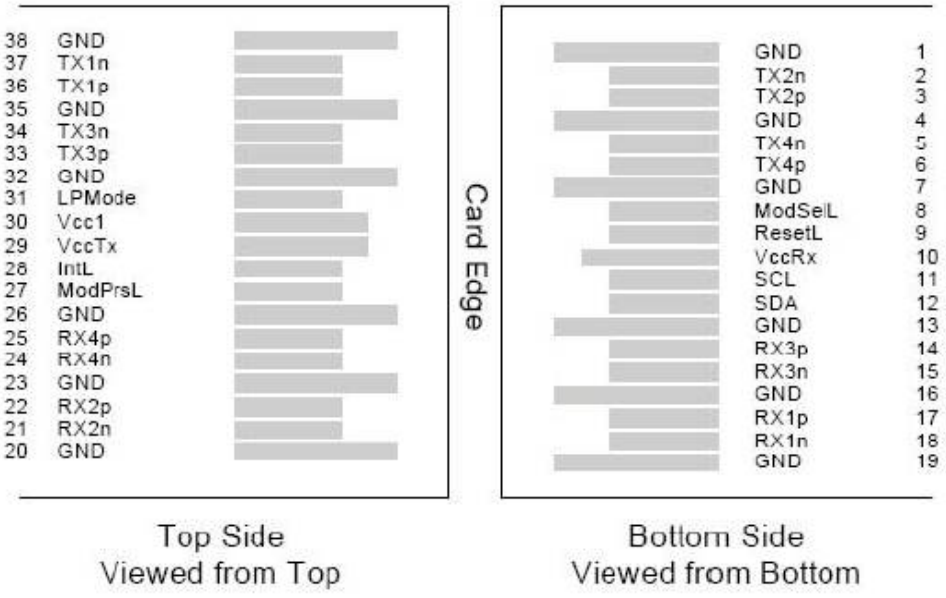
Parameter	Symbol	Min	Typ	Max	Units	Note
Storage Temperature	Tst	-30		80	°C	
Relative Humidity (non-	RS	-		85	%	

condensation)						
Operating Temperature	Topc	-5		75	°C	
Supply Voltage	VCC3	-0.3	3.3	3.6	V	
Voltage on LVTTL Input	Vilvttl	-0.3		VCC3 +0.2	V	

Normal operating condition

Parameter	Symbol	Min	Typ	Max	Units
Operating Temperature	Topc	-5		75	°C
Relative Humidity (non-condensation)	RS	-		85	%
Supply Voltage	VCC3	3.135	3.3	3.465	V
Power Supply Current	ICC3	750		-	mA
Total Power Consumption	Pd	-		2.0	W

QSFP Pin Assignments and Descriptions



Pin No.	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	

3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		Vcc Rx	+ 3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CMLO	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CMLO	Rx1p	Receiver Non-Inverted Data Output	
18	CMLO	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CMLO	Rx2n	Receiver Inverted Data Output	
22	CMLO	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CMLO	Rx4n	Receiver Inverted Data Output	1
25	CMLO	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTLO	ModPrsL	Module Present	
28	LVTTLO	IntL	Interrupt	

29		Vcc Tx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTLI	LPMode	Low Power Mode	
32		GND	Ground	1
33	CMLI	Tx3p	Transmitter Non-Inverted Data Input	
34	CMLI	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CMLI	Tx1p	Transmitter Non-Inverted Data Input	
37	CMLI	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Notes:

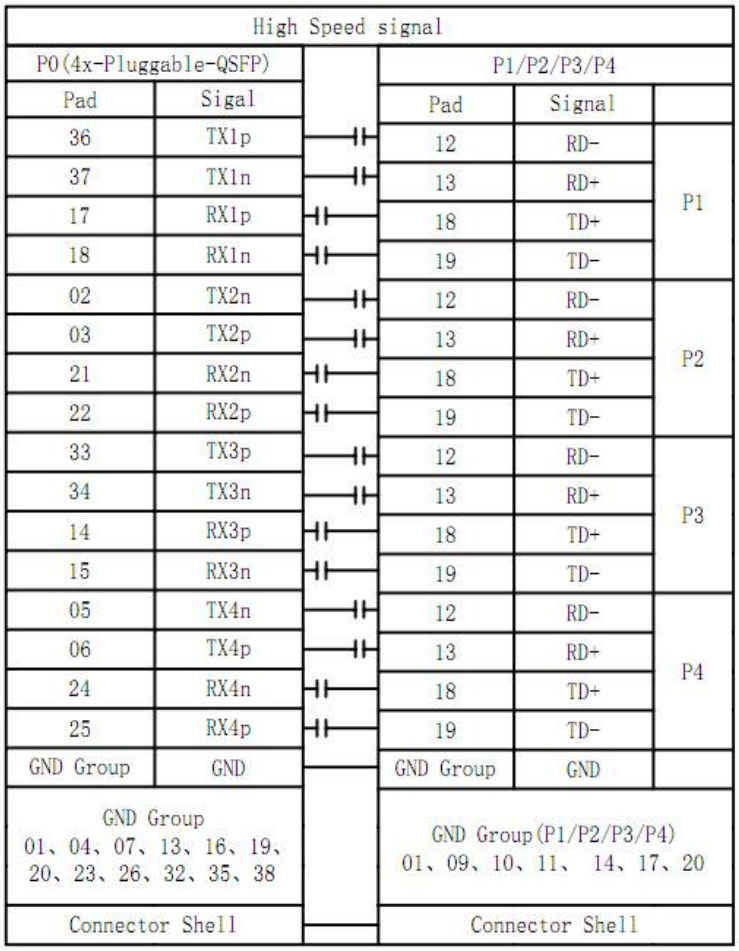
1. GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

SFP+ Pin Assignments and Descriptions

Pin No.	Logic	Symbol	Name/Description	Note
1		VeeT	Transmitter Ground	
2	LV-TTL-O	TX_Fault	N/A	
3	LV-TTL-I	TX_DIS	Transmitter Disable	
4	LV-TTL-I/O	SDA	Two Wire Serial Data	
5	LV-TTL-I	SCL	Two Wire Serial Clock	
6		MOD_DEF0	Module present, connect to VeeT.	
7	LV-TTL-I	RS0	N/A	
8	LV-TTL-O	LOS	LOS of Signal.	
9	LV-TTL-I	RS1		
10		VeeR	Receiver Ground	

11		VeeR	Receiver Ground	
12	CML-O	RD-	Receiver Data Inverted	
13	CML-O	RD+	Receiver Data NON-Inverted	
14		VeeR	Receiver Ground	
15		VccR	Receiver Supply 3.3V	
16		VccT	Transmitter Supply 3.3V	
17		VeeT	Transmitter Ground	
18	CML-I	TD+	Transmitter Data Non-Inverted	
19	CML_I	TD-	Receiver Data Inverted	
20		VeeT	Transmitter Ground	

Recommended Wiring Diagram



Low Speed Signal & Power		
P1(4x-Pluggable-QSFP)		
Pad	Signal	
08	Modsell	Vcc
09	Resetl	Vcc
10	VccRx	N.C.
11	SCL	Serial EEPROM Vcc
12	SDA	Serial EEPROM GND
27	ModPrsl	GND
28	Intl	Vcc
29	VccTx	Vcc
30	Vccl	
31	LpMode	N.C.

Low Speed Signal&Power		
P1/P2/P3/P4		
Pad	Signal	
02	TX_FAULT	TX_FAULT
03	TX_DISABLE	TX_DISABLE
04	MOD-DEF2	Serial EEPROM
05	MOD-DEF1	Serial EEPROM
06	MOD-DEF0	GND
07	RATESELE	GND
08	LOS	LOS
15	VCCR	Vcc
16	VCCT	

Mechanical Specifications